Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A processor, comprising:

a predicate predictor to determine a predicted predicate value and a confidence value for the predicted predicate value for a first instruction with a predicate; and

a micro-op generator to conditionally issue one or more micro-ops from a first or second set of unconditional micro-ops based on the predicted predicate value of said first instruction when said confidence value is high, wherein the first and second set of unconditional micro-ops correspond to conditional branches of said first instruction, and a sequence of micro-ops that implement the predicate of the first instruction without stalling the instruction when said confidence value is low.

2. (Currently Amended) The processor of claim 1, wherein each of said first or second set of unconditional micro-ops includes a check micro-op.

3. (Original) The processor of claim 2, wherein said check micro-op is to check for a calculated value of said predicate of true when said predicted predicate value is true.

4. (Original) The processor of claim 3, wherein said check micro-op is to initiate a recovery when said calculated value is false.

5. (Original) The processor of claim 3, wherein said first set of micro-ops includes a first micro-op corresponding to said first instruction without predicate.

6. (Original) The processor of claim 2, wherein said check micro-op is to check for a calculated value of said predicate of false when said predicted predicate value is false.

7. (Original) The processor of claim 6, wherein said check micro-op is to initiate a recovery when said calculated value is true.

8. (Previously Presented) The processor of claim 1, wherein said sequence of micro-ops includes a micro-op corresponding to said first instruction without predicate.

9. (Previously Presented) The processor of claim 8, wherein said sequence of micro-ops includes a conditional move micro-op.

10. (Currently Amended) A method, comprising:

determining a predicted predicate value for a first instruction with a predicate;

determining a confidence value for said predicted predicate value; and

issuing micro-ops corresponding to said first instruction responsive to said confidence value, wherein one or more micro-ops from a first or second set of unconditional micro-ops, wherein the first and second set of unconditional micro-ops correspond to conditional branches of said first instruction, are conditionally issued based on the predicted predicate value of said first instruction when said confidence value is high and a sequence of micro-ops that implement

the predicate of the first instruction without stalling the instruction when said confidence value is low.

11. (Currently Amended) The method of claim 10, wherein each of said first or second set of unconditional micro-ops includes a check micro-op when said confidence value is high.

12. (Original) The method of claim 11, wherein said check micro-op checks for a calculated value of said predicate of true when said predicted predicate value is true.

13. (Original) The method of claim 12, further comprising initiating a recovery when said calculated value of said predicate is false.

14. (Original) The method of claim 12, further comprising issuing a first micro-op corresponding to said instruction without predicate.

15. (Original) The method of claim 11, wherein said check micro-op checks for a calculated value of said predicate of true when said predicted predicate value is false.

16. (Original) The method of claim 15, further comprising initiating a recovery when said calculated value of said predicate is true.

17. (Currently Amended) The method of claim 10, wherein said ~~set~~ sequence of micro-ops includes a conditional move micro-op when said confidence value is low.

18. (Currently Amended) A system, comprising:

a processor including a predicate predictor to determine a predicted predicate value and a confidence value for said predicated predicate value for a first instruction with a predicate, and a micro-op generator to conditionally issue one or more micro-ops from a first or second set of unconditional micro-ops based on the predicted predicate value of said first instruction when said confidence value is high and a sequence of micro-ops that implement the predicate of the first instruction without stalling the instruction when said confidence value is low, wherein the first and second set of unconditional micro-ops correspond to conditional branches of said first instruction;

an interface to couple said processor to input-output devices; and

an audio input-output coupled to said interface and said processor.

19. (Currently Amended) The system of claim 18, wherein each of said first or second set of unconditional micro-ops includes a check micro-op.

20. (Original) The system of claim 19, wherein said check micro-op is to check for a calculated value of said predicate of true when said predicted predicate value is true.

21. (Original) The system of claim 20, wherein said check micro-op is to initiate a recovery when said calculated value is false.

22. (Original) The system of claim 21, wherein said first set of micro-ops includes a first micro-op corresponding to said first instruction without predicate.

23. (Original) The system of claim 19, wherein said check micro-op is to check for a calculated value of said predicate of false when said predicted predicate value is false.

24. (Original) The system of claim 23, wherein said check micro-op is to initiate a recovery when said calculated value is true.

25. (Previously Presented) The system of claim 18, wherein said sequence of micro-ops includes a micro-op corresponding to said first instruction without predicate.

26. (Previously Presented) The system of claim 25, wherein said sequence of micro-ops includes a conditional move micro-op.

27. (Currently Amended) An apparatus, comprising:

means for determining a predicted predicate value for a first instruction with a predicate;

means for determining a confidence value for said predicted predicate value; and

means for issuing micro-ops corresponding to said first instruction responsive to said confidence value, wherein one or more micro-ops from a first or second set of unconditional micro-ops, wherein the first and second set of unconditional micro-ops correspond to conditional branches of said first instruction, are conditionally issued based on the predicted predicate value of said first instruction when said confidence value is high and a sequence of micro-ops that implement the predicate of the first instruction without stalling the instruction when said confidence value is low.

28. (Currently Amended) The apparatus of claim 27, wherein each of said first or second set of unconditional micro-ops includes a check micro-op when said confidence value is high.

29. (Original) The apparatus of claim 28, wherein said check micro-op checks for a calculated value of said predicate of true when said predicted predicate value is true.

30. (Original) The apparatus of claim 29, further comprising means for initiating a recovery when said calculated value of said predicate is false.

31. (Original) The apparatus of claim 30, further comprising means for issuing a first micro-op corresponding to said instruction without predicate.

32. (Original) The apparatus of claim 28, wherein said check micro-op checks for a calculated value of said predicate of true when said predicted predicate value is false.

33. (Original) The apparatus of claim 32, further comprising means for initiating a recovery when said calculated value of said predicate is true.

34. (Currently Amended) The apparatus of claim 27, wherein said ~~set~~ sequence of micro-ops includes a conditional move micro-op when said confidence value is low.